REMARKS

This Amendment is in response to the Office Action dated October 25, 2001. Claims 1-9 and 11-14 are pending in the present application. Claims 1 and 8 have been amended, and claims 2, 3, 6, 9 and 13 have been cancelled. Accordingly, claims 1, 4, 5, 7, 8, 11, 12 and 14 are pending in the present application.

Amended Claims

Applicants have amended independent claim 1 to incorporate the limitations of claims 2, 3 and 6, while claim 8 has been amended to incorporate the limitations of claims 9 and 13. No new matter has been presented.

Objections to Disclosure

The Examiner objected to the Abstract because it was greater than 150 words. Applicants have amended the Abstract to bring it within 150 words.

35 U.S.C. § 112 Objection

The Examiner rejected claims 1-7 under 35 U.S.C. § 112, 2nd paragraph. The Examiner stated:

> Regarding claim 1, the claim recites the limitation of "the appropriate area", which is not defined by the Specification and seems to be a relative term.
> Regarding claim 2, the recitation of "the active area" lacks proper antecedent basis.
> Regarding claim 6, the recitation of "the source region and the drain region" lacks proper antecedent basis.

Claim 1 has been amended to delete reference to "the appropriate area" because as a halo

implant, one skilled in the art would know that such an implant, by definition, is targeted at the edges of the source and drain regions and slightly beneath the gate region separating the source and drain. Thus, reference to "the appropriate area" is not needed in claim 1. Moreover, the Specification discusses that the halo implant should be provided underneath the gate area in the targeted area designated by the shaded area in Figures 2 and 4. (Specification, page 5, lines 7-9). Accordingly, Applicants respectfully submit that claim 1, as now presented, satisfies the requirements of 35 U.S.C. §112.

As for claims 2 and 6, Applicants have amended claim 1 to incorporate the limitations of claims 2 and 6, and have provided proper antecedent basis for all elements. Claims 2 and 6 have been cancelled. Therefore, Applicants respectfully submit that the Examiner rejections under 35 U.S.C. §112 have been overcome.

35 U.S.C. § 103

In the Office Action, claims 1-9 and 11-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Specification in view of Hook et al. (U.S. Patent 6,083,794) ("Hook"). In so doing, the Examiner stated:

> Regarding claims 1, 7, 8 and 14, Applicant discloses a well-known method for providing a halo implant in a semiconductor device . . . . However, Applicant states that the art fails to teach a halo implant process wherein the thickness of the photoresist (213) is reduced. Hook et al. disclose that is well known in the art to provide a thin photoresist (18) be reducing the thickness (h). For instance see Figure 2, wherein Hook et al. teach that the reduction of the thickness (h) is given by:
>
> (1) $h=d\tan\theta$
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a thin photoresist. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of making multiple asymmetrical devices on a single common substrate at

different orthogonal orientations.

Regarding claims 2, 6, 9 and 13, Applicant discloses that the art fails to teach a photoresist that covers portions of source and drain regions. However, Hook et al. disclose that is well known in the art to place the photoresist at any point between the gate and a maximum distance (d), in which the source/drain regions are formed (see Figures 2-4).

The Examiner also rejected claims 1, 3-5, 7, 8, 11, 12 and 14 under 35 U.S.C. §103(a) as being unpatentable over Applicant's Specification in view of Chittipeddi et al. (U.S. Patent No. 5,045,486).

Applicants respectfully traverse. The present invention, as recited in claim 1, provides:

> 1. A method for providing a halo implant to a semiconductor device comprising the steps of:
>
> (a) providing a thin photoresist layer to the semiconductor device, wherein the thin photoresist layer is between approximately 0.1 to 0.2μm thick and covers a substantial amount of an active area comprising a source region and a drain region of the semiconductor device; and
>
> (b) providing the halo implant to the semiconductor device, wherein the thin photoresist layer is used as a mask.

Claim 8 is a system claim of similar scope to claim 1.

Turning first to Hook, Hook is directed to a process of manufacturing an asymmetrical semiconductor device. As part of the process, a vertical barrier is placed near a gate structure. The thickness or height (h) of the barrier casts an angled shadow which blocks an angled ion beam directed towards the side of the structure (see Figure 2). "The relationship between the height h of the barrier, the angle of the ion beam and the shadow being cast by the barrier is such that the mask for creating the barrier can be positioned with a much looser tolerance than would otherwise be required to produce an asymmetrical device." (Col. 2, lines 59-64).

In Hook, asymmetrical implantation is accomplished when the barrier is placed at one side of the gate structure in order to block implantation on the side of the gate closest to the barrier. Thus, the side of the gate furthest from the barrier, and not in its shadow, receives the

full implant dosage. (Col. 5, lines 25-28). In order to ensure asymmetrical implantation, the barrier must be placed within a distance d of the closest edge of the gate structure. The distance d is a function of the height (h) of the barrier and the implantation angle (θ). "The shallower the angle (θ) and the higher the barrier (h), the greater the tolerance of the position error in placing the barrier." (Col. 5, lines 33-35). Clearly, the opposite is also true --- the greater the angle of implantation and the thinner the barrier (h), the less the tolerance.

Hook fails to teach or suggest "providing a thin photoresist layer . . . between approximately 0.1 to 0.2 μm thick" to the semiconductor device, as recited in claims 1 and 8. In the present invention, reducing the thickness of a photoresist layer used to define a halo implant at the edges of a gate structure increases the accuracy of such an implant, which in turn, reduces counter doping in the source and drain regions. Hook makes no mention or suggestion of utilizing a *thin* barrier (photoresist) layer between approximately 0.1 to 0.2 μm thick, or reducing the height (h) of the barrier. Indeed, Hook suggests the contrary. Given the mathematical relationship between the height (h) of the barrier and the maximum distance (d) within which the barrier must be placed, the *thicker* the barrier (smaller the height), the greater the distance (d) becomes, assuming a constant implantation angle (θ). The greater the distance (d) becomes, the greater the tolerance for positioning error of the barrier, which in turn reduces the costs of implementation. (Col. 3, lines 24-29).

According to Hook, if the barrier height (h) was between approximately 0.1 to 0.2 μm thick, and the implantation angle was 45 degrees, then the maximum distance (d) the barrier may be placed is 0.1 to 0.2 μm from the side of the gate. The alignment accuracy of the mask used to form the barrier is "one half the sum of the width of the gate plus the maximum distance d." (Col. 3, lines 24-26). Thus, for today's technology standards where the gate width is

approximately 0.2 μm or less, the alignment accuracy of the mask must be within 0.2 μm. Thus, Hook teaches *away* from "providing a thin photoresist layer . . . between approximately 0.1 to 0.2 μm thick" to the semiconductor device, as recited in claims 1 and 8.

In addition, Hook fails to teach or suggest covering "a substantial amount of an active area comprising *a source region and a drain region*" with the thin photoresist layer, as recited in claims 1 and 8. As stated above, Hook is directed to producing an *asymmetric* semiconductor device. Accordingly, the barrier is used on only *one side* of the gate structure (see Figures 1 and 2). In other words, during an implant process, Hook's barrier covers on a portion of the source *or* drain, and *not* "a substantial amount of the an active area comprising a source region *and* a drain region," as recited in claims 1 and 8.

Accordingly, Applicants' Specification in view of Hook fails to teach or suggest the combination of elements disclosed in the present invention, as recited in claims 1 and 8. Applicants respectfully submit that claims 1 and 8 are allowable over the cited references. Claims 4, 5, 7, 11, 12 and 14 depend from claims 1 and 8, respectively, and therefore the above arguments apply with full force and effect to claims 4, 5, 7, 11, 12 and 14. Applicants respectfully submit that claims 4, 5, 7, 11, 12 and 14 are also allowable over the cited references.

Turning now to Chittipeddi, Chittipeddi is directed to a process for preventing ion channeling through a gate structure. In Chittipeddi, a layer of photoresist is deposited on top of the gate structure to protect the gate during ion implantation of the source and drain regions. To minimize shadowing from the gate structure, Chittipeddi teaches reducing the thickness of the photoresist layer to 2000 to 3000 Angstroms. (Col. 5, lines 12-18).

Chittipeddi fails to teach or suggest covering "a substantial amount of an active area comprising *a source region and a drain region*" with the thin photoresist layer, as recited in

claims 1 and 8. As shown in Figure 5 of Chittipeddi, only the gate structure 17 is covered by the photoresist layer 19. The photoresist layer 19 actually serves to define the gate structure in the proceeding process step (Col. 4, lines 55-58), which is left intact to protect the gate structure during the subsequent formation of the source and drain regions. Thus, Chittipeddi's photoresist layer does not cover "a substantial amount of an active area comprising *a source region and a drain region*," as recited in claims 1 and 8.

In addition, Chittipeddi fails to teach or suggest using the thin photoresist layer "as a mask" for the halo implant. As stated above, the photoresist layer serves to protect the gate structure during ion implantation of the source and drain regions (col. 5, lines 6-12). At most, the photoresist layer is a mask for the source and drain regions. Unlike the present invention, however, Chittipeddi's photoresist layer is not a mask for the halo implant.

Accordingly, Applicants' Specification in view of Chittipeddi fails to teach or suggest the combination of elements disclosed in the present invention, as recited in claims 1 and 8. Applicants respectfully submit that claims 1 and 8 are allowable over the cited references. Claims 4, 5, 7, 11, 12 and 14 depend from claims 1 and 8, respectively, and therefore the above arguments apply with full force and effect to claims 4, 5, 7, 11, 12 and 14. Applicants respectfully submit that claims 4, 5, 7, 11, 12 and 14 are also allowable over the cited references.

Conclusion

In view of the foregoing, it is submitted that claims 1, 4, 5, 7, 8, 11, 12 and 14, as now presented, are allowable over the cited references and are in condition for allowance. Applicants respectfully request reconsideration of the rejections and objections to the claims.

Applicants' attorney believes that this application is in condition for allowance. Should

any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Attached hereto and captioned "**Version with Markings to Show Changes Made**" is a marked-up version of the changes made to the specification and the claims by the current amendment.

Respectfully submitted,

January 21, 2002

Joyce Fom
Sawyer Law Group LLP
Attorney for Applicant(s)
Reg. No. 48,681
(650) 493-4540

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Once Amended) A method for providing a halo implant to a semiconductor device comprising the steps of:

(a) providing a thin photoresist layer to the semiconductor device, wherein the thin photoresist layer is between approximately 0.1 to 0.2μm thick and covers a substantial amount of an active area comprising a source region and a drain region of the semiconductor device; and

(b) providing the halo implant to ~~the appropriate area of~~ the semiconductor device, wherein the thin photoresist layer is used as a mask.

8. (Twice Amended) A system for providing a halo implant to a semiconductor device comprising:

means for providing a thin photoresist layer to the semiconductor device, wherein the thin photoresist layer is between approximately 0.1 to 0.2μm thick and covers a substantial amount of an active area comprising a source region and a drain region of the semiconductor device; and

means for providing the halo implant to the semiconductor device, wherein the thin photoresist layer is used as a mask.

IN THE ABSTRACT

A method and system for providing a halo implant to a semiconductor device is disclosed. The method and system comprises providing a thin photoresist layer between approximately 0.1 to 0.2μm thick to the semiconductor device, wherein the thin photoresist layer covers a substantial

amount of an active area comprising a source region and a drain region of the semiconductor device. The method and system further includes providing the halo implant to the to the semiconductor device, using the thin photoresist layer as a mask~~appropriate area of the semiconductor device~~. ~~Accordingly, in a system and method in accordance with the present invention, a photoresist that is capable of thinner profile, i.e., DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows.~~

~~With~~ Utilizing this thin photoresist ~~thickness~~ layer, taking into account other height variables, the source and drain regions can be opened only as needed. At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. ~~This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.~~

~~In the smaller geometries of 0.18 um technologies and lower, the gate height will actually work to advantage and help reduce unwanted counter doping of the source/drain area. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries.~~